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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,055	07/25/2003	Ryoji Suzuki	9792909-5648	2206
26263	7590	10/10/2006	EXAMINER	
SONNENSCHEIN NATH & ROSENTHAL LLP			TRAN, NHAN T	
P.O. BOX 061080			ART UNIT	PAPER NUMBER
WACKER DRIVE STATION, SEARS TOWER				
CHICAGO, IL 60606-1080			2622	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/627,055	SUZUKI ET AL.
	Examiner Nhan T. Tran	Art Unit 2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 7/25/2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 27 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 27 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 25 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 09/134,153.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/134,153, filed on 8/14/1998.

Drawings

2. Figure 15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. Preliminary amendments to title and related application data of specification filed 7/25/2003 are acknowledged and accepted.

Double Patenting

(An Important note: This application is a voluntary division of the parent application No. 09/134,153 filed 8/14/1998, which is now US Patent No. 6,677,993. No restriction was made by the USPTO in the parent application. Thus, prohibition of double patenting rejections under 35 USC 121 does not apply. See MPEP 804.01.)

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 27 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2 & 5 of U.S. Patent No. 6,677,993 B1 in view of Akimoto et al. (US 4,942,474).

All limitations of the instant claim 27 for a solid-state image sensor are broader in every aspect than the patent claims 1, 2 & 5 except for the limitations of "a vertical

scanning circuit for controlling said amplifying element.” It should be noted that the instant claim “a reset element” is encompassed by a reset circuit of the patent claims 1, 2 & 5 in which a horizontal scanning circuit is also the reset circuit for controlling resetting of unit pixels per column.

Although the patent claims 1, 2 & 5 do not teach “a vertical scanning circuit for controlling said amplifying element”, the patent claim 2 teaches that the image sensor is a two-dimensional pixel arrays comprising rows and columns. In another reference to **Akimoto**, a two-dimensional solid-state image sensor having rows and columns of pixels is taught, wherein each pixel is implemented with a pixel amplifier element (transistor 4 shown in Figs. 3 & 4) which is controlled by a vertical scanning circuit (21) via at least a signal line (a signal line 45 in Fig. 3 or a signal line 7 in Fig. 4). In both cases of Fig. 3 and Fig. 4 in Akimoto, the vertical scanning circuit (21) is essential for controlling pixel amplifiers (4) by accessing to each row of pixels of the two-dimensional image sensor to properly and timely control the output of each pixel amplifier so that an amplified signal from each pixel is outputted to an output line in a predetermined order of conventional fashion. See Akimoto, col. 2, line 54 – col. 3, line 24 and col. 5, lines 1-8.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the patent claims 1, 2 & 5 of the U.S. Patent No. 6,677,993 B1 a vertical scanning circuit for controlling the amplifying element by accessing to each row of unit pixels as an essential control feature of the two-

dimensional solid-state image sensor in a balanced design so that signal charges would be properly and timely amplified and outputted for further processing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Akimoto et al. (US 4,942,474).

Regarding claim 27, Akimoto discloses a solid-state image sensor (Fig. 3, col. 2, line 54 – col. 3, line 24) comprising:

a photoelectric conversion element (photodiode 1; Fig. 3, col. 2, lines 56-60) for converting incident light into an electric signal charge;

an amplifying element (pixel amplifier 4; Fig. 3, col. 2, lines 60-64) for amplifying an electric signal from said photoelectric conversion element;

a reset element (reset switch 3; Fig. 3, col. 2, lines 60-64) for resetting said photoelectric conversion element;

a select switch (read-out switch 47; Fig. 3) for selectively outputting the electric signal as a pixel signal from said amplifying element to a signal line (signal line 48) (see col. 2, line 67 – col. 3, line 1);

a vertical scanning circuit (vertical scanning circuit 21; Fig. 3) for controlling said amplifying element (see col. 2, line 54 – col. 3, line 24, wherein the input and output of the pixel amplifier 4 are controlled by the vertical scanning circuit 21 through transistors 2 and 47 by signal lines 5, 45 and a signal line connected at the gate of transistor 47. Note in Fig. 3 that the pixel amplifier 4 is controlled to output an amplified signal when at least the output of the pixel amplifier 4 is turned ON by the vertical scanning circuit via signal line 45 and the gate of transistor 47 (ON state) so that the signal charge is properly and timely amplified and read out);

a horizontal scanning circuit (horizontal scanning circuit 22) for controlling said reset element (see Fig. 3; col. 2, line 54 – col. 3, line 24, wherein reset switch 3 is controlled by the horizontal scanning circuit 22 via line 52).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Akimoto et al. US 4,809,075

Yonemoto et al. US 6,801,253

Shinohara et al. US 5,698,844

Tanaka et al. US 6,037,577

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NT.

Nhan T. Tran
Patent Examiner



DAVID OMETZ
SUPERVISORY PATENT EXAMINER